> a delay controller, coupled to receive at least one of the delay more signal or the delay less signal, for generating an adjusting signal to adjust the delays of each data strobe signal;
>
> a first delay element, coupled to receive a source data strobe signal and the adjusting signal from the delay controller, for generating the second data strobe signal;
>
> a second delay element, coupled to receive the first data strobe signal and the adjusting signal from the delay controller, for generating the first data strobe signal; and
>
> a third delay element, coupled to receive the second data strobe signal and the adjusting signal from the delay controller, for generating the third data strobe signal.

In addition, Applicant has amended claim 6 to now recite a method for ensuring the capture of valid data, the method including:

> . . .
>
> adjusting each data strobe signal individually to delay more in response to the latched data from the first latch and the second latch being not equal;
>
> comparing the latched data from the second latch and the third latch to determine if the latched data is equal; and
>
> adjusting each data strobe signal individually to delay less in response to the latched data from the second latch and the third latch being not equal.

The claimed invention defines a system and a method that guarantees data capture. Moreover, the claimed invention guarantees data capture at high operating frequencies and at high system temperatures. This beneficially increases system performance because there are no delays associated with capturing data at any particular clocking interval. Further, the claimed invention advantageously provides a system and a method that eliminates the requirement of programming a data capture system at particular intervals for adjustments to account for inconsistent chip voltages or chip temperatures that cause delays or data drift.

The claimed invention is neither disclosed nor suggested by Doi, either alone or in combination. Doi discloses controlling clock timing by detection of a deviation of the clock timing from a desired reference timing and then using the result of the detection to apply feedback to the clock generator. Doi, col. 1, lines 62-66. Doi discloses an error discriminator 508 that generates an error discrimination signal for a delay circuit 510. The signal is received ***only*** by the initial delay circuit 510 in a clock generator. This is the only delay that can be varied and subsequent delay stages 511, 512 must remain fixed with respect to the initial delay stage. Col. 5, lines 59-65; Figure 7. Therefore, any errors in the initial delay circuit are also propagated and cannot be corrected so that data ultimately cannot be reliably captured.

By contrast, the claimed invention uses a delay control circuit to ***separately*** apply an adjustment signal to ***each*** individual delay block. By applying a separate delay to each individual delay block, each delay block includes at least two variables to individually generate a data strobe signal. Each generated data strobe signal may then be used to properly capture valid data because adjustments necessary to account for any data drift are accounted for in each delay stage. This guarantees valid data capture. Thus, Applicant respectfully submits that Doi does not disclose or suggest the invention as is now claimed.

In addition, claims 3-5 provide additional novel features of the claimed invention in claim 1, and are also patentably distinguishable over Doi. For example, the delay counter includes an "OR latch for generating a software interrupt signal" in response to receiving certain signals to increase or decrease delays. Similarly, claim 7 provides additional novel features of the claimed invention in claim 6, and is also patentably distinguishable over Doi.

For example, claim 7 recites "generating a qualified delay more signal" and "generating a qualified delay less signal" in response to some appropriate threshold value being exceeded.

Applicant respectfully submits that claims 1 and 3-7, as amended herein, are patentably distinguishable over the cited references (including references cited, but not applied). Therefore, Applicant requests reconsideration and allowance of claims 1 and 2-7, as amended herein. In addition, Applicant respectfully submits that new claim 8 provides additional novel features of the invention in claim 1 and is also patentably distinguishable over the cited references.

Respectfully submitted,
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